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Reduced Contact Resistance in Inkjet Printed High-Performance Amorphous Indium Gallium Zinc Oxide Transistors

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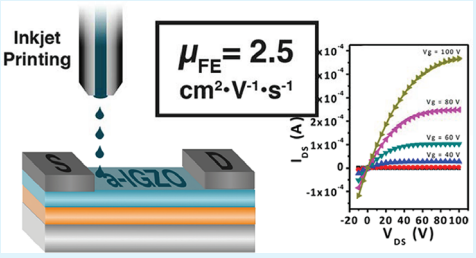
Supporting Information

ABSTRACT: Solution processing of amorphous metal oxide materials to fabricate thin-film transistors (TFTs) has received great recent interest. We demonstrate here an optimized "ink" and printing process for inkjet patterning of amorphous indium gallium zinc oxide (a-IGZO) TFTs and investigate the effects of device structure on derived electron mobility. Bottom-gate top-contact (BGTC) TFTs are fabricated and shown to exhibit electron mobilities comparable to a-Si:H. Furthermore, a record electron mobility of 2.5 $cm^2\ V^{-1}\ s^{-1}$ is demonstrated for bottom-gate bottom-contact (BGBC) TFTs. The mechanism underlying such impressive performance is investigated using transmission line techniques, and it is shown that the semiconductor-source/drain electrode interface contact resistance is nearly an order of magnitude lower for BGBC transistors versus BGTC devices.



KEYWORDS: *thin-film transistor, metal oxide semiconductor, inkjet printing, transparent electronics, contact resistance, device structure*

INTRODUCTION

Electronic circuitry based on optically transparent semiconductors is of great current interest in applications such as large area liquid-crystal displays, organic light-emitting diode displays, energy-saving smart windows, radio frequency identification tags, and sensors.[1−5] For recent reviews of this field, see ref 6−11.[6−11] Indeed, major progress has been made recently in the integration of amorphous oxide semiconductors (AOS) in thin film transistors (TFTs) for large area display backplane and transparent circuits. Various metal oxide semiconductors have been investigated, including, In_2O_3,[12] SnO_2,[13] ZnO,[14−16] ZTO,[17,18] IZO,[19] ZITO,[20−22] HIZO,[23] and IGZO.[24−29] The high electron mobilities in these amorphous materials have been attributed to conduction pathways composed of the highly delocalized *n*s-states of the metal ions having filled d-shell configurations, which suppress optical absorption by limiting d−d interband transitions.[30−32] In comparison to the relatively small sp^3-orbital overlap in amorphous covalent semiconductors (e.g., Si, GaAs), the spatial expanse of s-orbitals in atoms with $(n-1)d^{10}ns^0$ ($n \geq 5$) electron configurations affords AOS electron mobilities remarkably comparable to those of the corresponding crystalline phases.[26] In terms of vapor-phase grown thin films, the amorphous quaternary system indium gallium zinc oxide (a-IGZO) has been of particular interest because of the substantial electron mobilities (>10 $cm^2\ V^{-1}\ s^{-1}$), large current on/off ratios ($\geq 1 \times 10^7$), as well as light and bias stability superior to that of a-Si:H.[60] Interest in this material is heightened by the recent report of a 37 in. active matrix liquid crystal display (AM-LCD), a 6.5 in. flexible AM-OLED display, and a 14.1 in. transparent OLED display based on IGZO TFT driving electronics.[33] In a-IGZO, the primary conduction pathway is provided by In^{3+} s-states, whereas the strong Ga^{3+} oxygen affinity suppresses oxygen vacancies and tunes the carrier concentration. In addition, Zn^{2+} introduces cation size variation in the structure which helps to stabilize the amorphous phase.[34]

To date, the majority of IGZO research has focused on vapor-phase growth techniques such as pulsed laser deposition (PLD),[26] radio frequency magnetron sputtering,[35] and direct-current sputtering.[36] However, solution processing offers an attractive means to minimize manufacturing costs,[37] and oxide semiconductor growth methods used have included chemical bath deposition,[38] drop-casting,[39] spin-coating,[27,40,41] and inkjet printing.[42−46] Among these, inkjet printing is particularly attractive because of the low material waste and the ability to print complex patterns, eliminating costly masking steps.[47] Thus far, few systematic studies have been reported utilizing inkjet printing to fabricate IGZO TFTs.[43,45,46] In those studies, G. Kim et al. demonstrated polycrystalline IGZO with a low mobility of 0.03 $cm^2\ V^{-1}\ s^{-1}$, whereas D. Kim et al. and Wang

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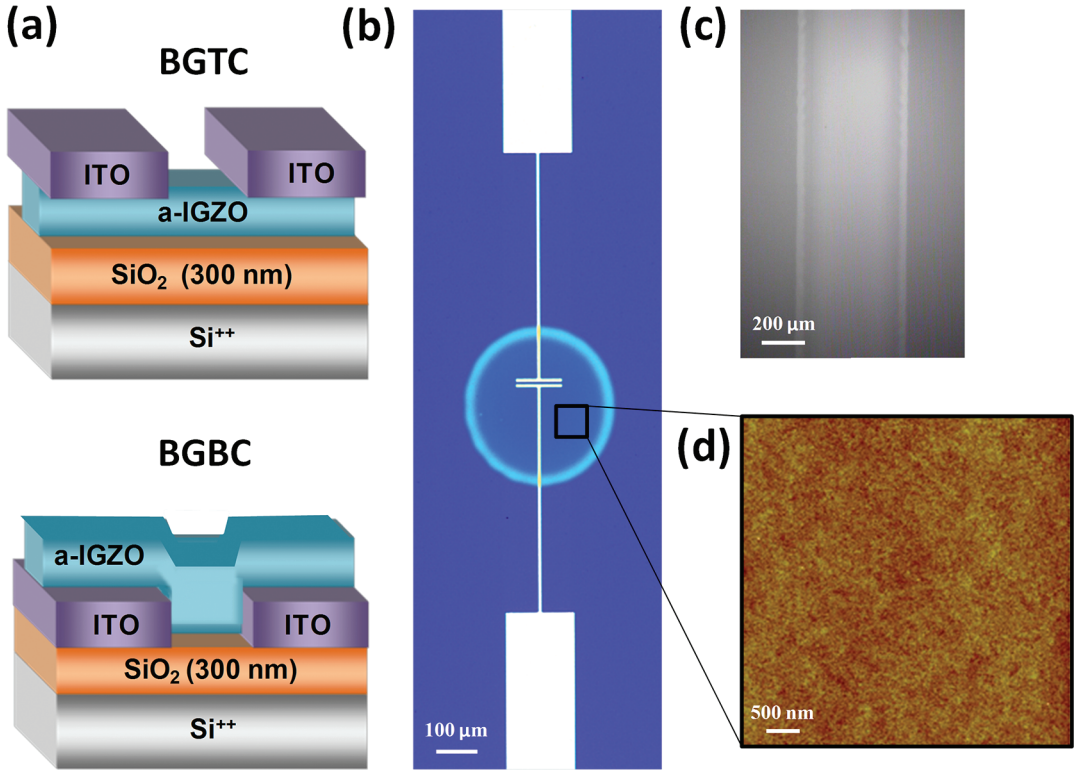

Figure 1. (a) TFT device architecture. (b) Optical microscope images of a printed IGZO droplet on an ITO electrode and (c) line. (d) AFM of smooth IGZO surface.

et al. varied the channel layer thickness and obtained maximum mobilities of 0.05 $cm^2\ V^{-1}\ s^{-1}$ and 1.41 $cm^2\ V^{-1}\ s^{-1}$, respectively. Very recently, Jeong et al. reported field-effect mobilities as high as 7.6 $cm^2\ V^{-1}\ s^{-1}$ for printed IGZO TFTs having ITO electrodes and a channel width (W)/length (L) ratio of 1.0.[48] As discussed below, selection of this ratio is crucial for deriving meaningful mobilities.[49] Here we investigate the effects of transistor architecture and semiconductor/electrode contact resistance on the performance of inkjet-printed a-IGZO TFTs. Specifically, we demonstrate bottom-gate bottom-contact TFTs (W/L = 10−30 or defined) exhibiting mobilities as high as 2.45 $cm^2\ V^{-1}\ s^{-1}$ for channel lengths of 50 μm, and show that this substantial mobility reflects very low contact resistance at the electrode-semiconductor interface. This is the highest mobility reported to date for a printed a-IGZO TFT with realistic channel dimensions.

EXPERIMENTAL SECTION

Device Fabrication. TFT devices were fabricated on p^+-Si/SiO_2 (300 nm thermal oxide; Montco Silicon Technologies Inc.) cleaned by sonication for 2 min in ethanol, dried under an N_2 flow, and treated with an oxygen plasma for 5 min prior to inkjet printing. Reagents for preparing inkjet "inks" were purchased from Sigma-Aldrich Chemicals and used without further purification. Gallium nitrate hydrate (99.999%), indium nitrate hydrate (99.999%), and zinc acetate dihydrate (99.99%) with a In:Ga:Zn 57:12:31 mol ratio were dissolved in 2-methoxyethanol to 0.32 M total metal concentration. Monoethanolamine (0.1 M) was added to aid in solubilizing the metal salts. The solution was stirred at 80 °C for 40 min in order to fully dissolve the metal salts, allowed to age for 3 h at 25 °C to aid hydrolysis,[50] and then filtered through a 0.45 μm PTFE membrane prior to printing.

Oxide TFT features were printed with a Dimatix 2800 Materials Printer using a surface-to-print-head distance of 0.6 mm with 7 nozzles maintained at 56 °C. The substrate surface was maintained at 60 °C to facilitate uniform droplet spreading. We found that lower nozzle temperatures lead to nonuniform and inconsistent printed features. Droplet size was measured to be ~450 μm using the Dimatix on-board camera. Postdeposition annealing was performed at 300 or 400 °C on a hot plate in air for 30 min. The optimal "ink" decomposition temperature was determined by thermogravimetric analysis performed on a Shimadzu-TGA 50 instrument. Shipley 1813 positive photoresist was deposited by spin-coating at 5000 rpm for 40 s and soft-baked at 110 °C for 1 min. An exposure of 96 mJ was delivered by a Süss MABA6 Mask Aligner with a mask affording channel dimensions of 100 or 1000 μm (W) × 3, 6, 10, and 50 μm (L), and subsequently developed using Shipley 352 developer. ITO source/drain electrodes (99.99%, In:Sn = 9:1; from Williams Advanced Materials Inc.) were deposited by IAD at room temperature using a previously reported method.[51] Photoresist lift-off was performed by sonication in acetone for 5 min.

Device Characterization. Film thickness and surface roughness were measured by a Veeco Dektak 150 surface profiler and a Veeco ICOP PT atomic force microscope in tapping-mode with silicon cantilevers (Applied NanoStructures, Inc.). ITO sheet resistance was measured using a Fluke FLU-87−5 digital multimeter. Transfer and output measurements were made with a Signatone probe station with a Keithley 6430 subfemtoamp remote source meter and a Keithley 2400 source meter using locally written LabVIEW software. All electrical characterizations were carried out in ambient with no intentional light blocking.

RESULTS AND DISCUSSION

Inkjet Printing Optimization. Prior to TFT fabrication, IGZO ink formulations were optimized for inkjet printing from those previously reported for spin-coating.[27] The total metal concentration in 2-methoxyethanol was 0.32 M with a In:Ga:Zn molar ratio of 57:12:31 and with 0.1 M monoethanolamine as a stabilizing agent. By varying the printer nozzle-head temperature, jetting speed, droplet size, and substrate temper-

ature, controlled droplets and lines are readily deposited (Figure 1 below).

Evidence of "coffee-stain effects" can be observed in both the printed drops and lines. This results from capillary action which forces outward flow of the drying ink, thus depositing larger amounts of material at the edge of the drop.[52] Although this artifact can have deleterious effects in dense, complex TFT circuits (by transferring ink beyond the source-drain electrodes), we find that by selecting appropriate drop size and controlling the surface affinity for the ink, the effect is negligible on single TFT performance (vide infra). Indeed, atomic force microscopy (AFM) of the central film section reveals extremely smooth IGZO surfaces with typical rms roughnesses of 0.32 nm and a droplet/line thickness of ~15 nm as measured by profilometry.

Thin-Film Transistor Device Fabrication and Characterization. Using the above film patterning/growth conditions, both bottom-gate/bottom-contact (BGBC) and bottom-gate/top-contact (BGTC) TFTs are readily fabricated. Highly doped p^+-Si/SiO_2 (300 nm thermal oxide, C_i = 11 nF/cm^2) wafers served as the substrate/gate electrode and gate insulator on which 50 nm thick ITO electrodes were deposited by ion-beam assisted deposition (IAD) before (for BGBC TFTs) or after (for BGTC TFTs) semiconductor film deposition. Subsequent ITO patterning using standard lift-off procedures results in devices with channel lengths (L) of 3, 5, and 10 μm with channel widths (W) of 100 μm, as well as in devices with L = 50 μm and widths defined by the printed drop size (see Experimental Section for more details). Channel dimensions were carefully chosen to ensure negligible fringing electric fields by maintaining $W/L > 10$.[49] Furthermore, for devices with L = 50 μm, the selection of an electrode larger than the printed drop size defined the channel width as the drop diameter (measured individually by optical microscopy). IAD is a highly versatile, two-beam sputtering technique that enables the growth of smooth (rms roughness <1 nm) and highly conductive (sheet resistance ~125 $\Omega\ \square^{-1}$) ITO thin films at room temperature.[51,53−55] Both conductivity and crystallinity can be controlled by varying ion beam energy, ion current density, and Ar/O_2 gas flow rates. Utilizing optimized inkjet printing conditions, drops of ~450 μm diameter were printed on oxygen plasma cleaned substrates and then annealed at 300 or 400 °C. These temperatures were selected on the basis of a previous study[27] demonstrating that thermally driven M−OH + HO−M condensation is the limiting step in oxide lattice formation and in oxygen-vacancy generation. These processes were shown to be complete for IGZO by 400 °C, however, here we also investigated processing at 300 °C because this temperature lies below the glass transition temperature of plastic substrates attractive for flexible electronics.[56]

Representative transfer and output plots for both BGBC and BGTC TFTs with channel lengths of 10 μm and annealed at 400 °C are shown in Figure 2, whereas additional plots are reported in the Supporting Information. Gate current (i.e., gate leakage) is also plotted alongside the transfer curves, demonstrating minimal contribution to I_{DS}. Because these devices were fabricated on relatively thick SiO_2 dielectrics, operating voltages of 100 V were used for all electronic characterizations. To analyze the details of a-IGZO TFT performance, we evaluated field-effect mobility (μ_{FE}), threshold voltage (V_T), and current on/off ratio (I_{on}:I_{off}), and all results are collected in Table 1 below. From these data, several important conclusions can be drawn. First, inkjet printed

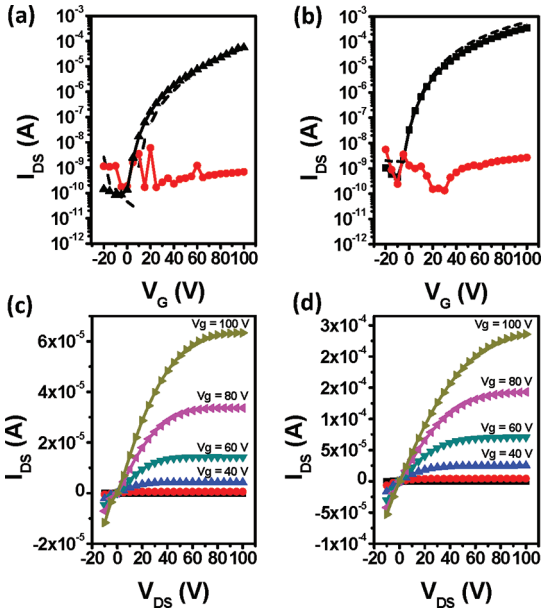

Figure 2. (a, b)Typical transfer and (c, d) output characteristics for (a, c) BGTC and (b, d) BGBC TFTs. Transfer plots show very low gate leakage (red).

BGTC devices exhibit device performance comparable to that of BGTC devices fabricated by previously reported spin-coating techniques.[27] Second, after 400 °C annealing, the performance of these printed a-IGZO devices rivals or exceeds that of typical a-Si:H based TFTs.[57] These results demonstrate that inkjet printing of a-IGZO TFTs is a viable materials-efficient approach versus conventional spin-coating.

In all of the present devices, the apparent mobility is found to fall as the channel length decreases, and this is not unexpected.[58] For example, in vapor-deposited a-IGZO TFTs, the channel length (L) was varied while maintaining a constant width/length ratio (W/L) and the contact resistance (R_C) then calculated. This analysis reveals that for channels with small L (<10 μm), non-Ohmic contacts result from non-negligible contact resistance which is shown to have a greater effect as L is decreased. A comparison of W/L = 400 μm/20 μm with W/L = 50 μm/2.5 μm at 10 V gate bias reveals a reduction in I_{DS} and μ_{FE} from 0.24 mA and 7 cm^2 V^{-1}s^{-1} to 0.10 mA and 4 cm^2 V^{-1} s^{-1}, respectively. Finally and most interestingly, the present BGBC TFTs exhibit field-effect mobility values as high as 2.45 cm^2 V^{-1} s^{-1} (T_A = 400 °C, W/L (defined) = 450/50), which is significantly greater than any previously reported mobility for inkjet printed a-IGZO TFTs (1.4 cm^2 V^{-1} s^{-1}, T_A = 500 °C, W/L = 200/200 μm[43,45,46]), despite the lower annealing temperatures and channel lengths used here. The relatively large threshold voltages measured in this study likely reflect the high operating voltages (100 V) necessary for the thick, low capacitance SiO_2 dielectric used (300 nm),[59] and the relatively thin a-IGZO layer.[45] Future work with thin, high-κ dielectrics and encapsulating layers will address this issue.

Contact Resistance Measurements. To elucidate the origin of the present large mobility enhancements, contact resistance measurements were performed using the transmission line method.[61] At low V_{DS}, the total resistance of a

Table 1. Performance Metrics for TFTs Fabricated by Inkjet Printing a-IGZO with Either a BGTC or BGBC Structure at Various Annealing Temperatures

device architecture−annealing temperature	L (μm)	W^a (μm)	μ_{FE} (cm^2V^{-1} s^{-1})	V_T (V)	I_{on}:I_{off}	$R_C{}^b$ (Ω cm)
top-contact−400 °C	3	100	0.12	18.2	4.0×10^6	2.29×10^3
	6	100	1.04	33.1	6.0×10^6	
	10	100	1.17	33.1	6.0×10^6	
	50	~450, defined	1.30	17.4	5.0×10^6	
bottom-contact−400 °C	3	100	0.61	29.5	6.0×10^6	
	6	100	1.10	34.3	5.0×10^5	3.66×10^2
	10	100	2.06	28.4	8.0×10^5	
	50	~450, defined	2.45	21.9	9.0×10^5	
top-contact−300 °C	3	100	0.06	44.2	3.0×10^4	1.01×10^4
	6	100	0.14	46.4	3.0×10^4	
	10	100	0.18	48.7	4.0×10^4	
	50	~450, defined	0.21	43.0	4.0×10^4	
bottom-contact−300 °C	3	100	0.09	43.8	8.0×10^5	2.79×10^3
	6	100	0.26	41.3	2.0×10^6	
	10	100	0.43	38.8	2.0×10^6	
	50	~450, defined	0.48	40.9	9.0×10^5	

[a]To ensure negligible fringing electric fields for devices with L = 50 μm, the selection of an electrode larger than the printed drop size defined the channel width as the drop diameter (measured individually by optical microscopy). [b]Contact resistance, R_C, calculated at 100 V source/drain bias.

TFT, R_T, can be defined by eq 1, where $r_{ch}L$ is the channel resistance per unit

$$R_T = \frac{V_{DS}}{I_{DS}} = r_{ch}L + R_C \quad (1)$$

length and R_C is the contact resistance at the semiconductor/electrode interface. To determine R_C, output plots were taken from devices with varying channel lengths, fabricated on the same chip to ensure materials consistency. When the inverse of the slope at low V_{DS} is then plotted against channel length L, the y-intercept gives R_C . Figure 3a shows a representative plot

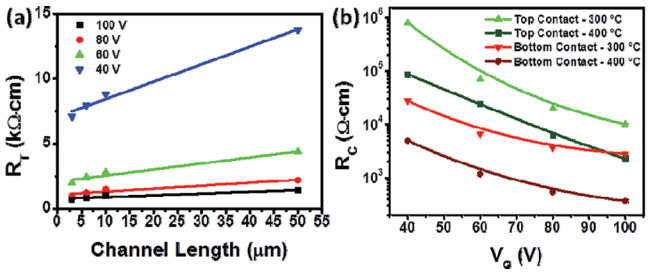

Figure 3. (a) Total measured resistance as a function of channel length at various applied V_G values for BGBC, 400 °C annealed, printed IGZO TFTs. (b) Dependence of the extracted contact resistance (R_C) on gate voltage (V_G) for IGZO TFTs with BGBC (red) and BGTC (green) structure annealed at 300 °C (light) or 400 °C (dark).

of R_T versus L data, and Figure 3b plots the contact resistance of BGTC and BGBC TFTs at both annealing temperatures versus applied gate voltage.

For all of the present devices, R_C decreases with increasing applied bias to the gate. Furthermore, a significant reduction in R_C is observed for the BGBC versus BGTC TFT configuration. This reduction is likely caused by coannealing/interdiffusion of the ITO electrode with the IGZO overlayer. That is, in top-contact devices, IGZO is printed and then annealed, followed by photolithography to deposit the ITO electrodes. However, in the bottom-contacted devices, the ITO electrodes are patterned first, followed by IGZO printing, and finally the two oxides are annealed together. Furthermore, several additional benefits can arise from the coannealing of the ITO electrodes and the IGZO interlayer. First, the ITO deposited by IAD has been previously demonstrated to exhibit enhanced conductivity after thermal treatment.[54] Second, whereas the improvement in mobility and R_C with increasing annealing temperature for BGTC devices is due to only thermally driven condensation, leading to greater oxide-lattice formation,[27] in BGBC devices, the IGZO ink undergoes oxide-lattice formation in intimate contact with the ITO electrodes, improving the semiconductor/electrode interface. This dual improvement mechanism for BGBC devices can also explain why BGBC TFTs annealed at 300 °C exhibit R_C values nearly as low as in BGTC TFTs annealed at 400 °C. Barquinha and co-workers reported slight interdiffusion at the electrode/semiconductor interface using TOF-SIMS when IGZO was coannealed with various electrode materials.[62] Although their work did not focus on ITO electrodes, they demonstrated that such interdiffusion results in significant μ_{FE} increases using Ti/Au source/drain electrodes. The present observation of low contact resistance in BGBC a-IGZO/ITO TFTs is in agreement with these results.

CONCLUSIONS

In summary, a-IGZO deposition by inkjet printing has been optimized and TFTs fabricated and characterized. Bottom-gate/top-contact devices annealed at 400 °C show μ_{FE} up to 1.30 cm^2 V^{-1} s^{-1}, V_T as low as 17 V, and I_{on}:I_{off} > 1×10^6 — all parameters comparable to spin-coated a-IGZO. In contrast, bottom-gate/bottom-contact TFTs exhibit a record $\mu_{FE} \approx 2.45$ cm^2 V^{-1} s^{-1}, acceptable $V_T \approx 22$ V, and I_{on}:$I_{off} \approx 1 \times 10^6$. The low contact resistance in the bottom-contact structure is likely due to interfacial interdiffusion of the semiconductor and ITO electrode during annealing, which accounts for the enhanced mobility. Future work will include introducing high-κ gate dielectrics to lower operating voltages and further increase field-effect mobilities.[63]

■ ASSOCIATED CONTENT

Supporting Information

Thermogravimetric analysis of the a-IGZO precursor ink and additional transfer and output plots. This material is available free via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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